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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,431	12/20/2004	Yuichi Okuda	HITA.0652	6767

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EXAMINER	
LE, TOAN K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/518,431	OKUDA, YUICHI	
	Examiner	Art Unit	
	Toan Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-3,7,8,10-12 and 15-22 is/are rejected.

7)☒ Claim(s) 4-6,9,13 and 14 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 December 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/20/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: East search history .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. This office acknowledge receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on December 20, 2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. Claim 1 is objected to because of the following informalities:

In claim 1, lines 5-6, "the internal circuit" will be understood as -- an internal circuit --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 7-8, 10-12 and 15-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hansen et al. (US. 5,778,419).

Regarding claim 1, Hansen et al. disclose in Figs. 1 and 5, A semiconductor integrated circuit device having: an input terminal (input port 110 of fig. 1) for receiving an input signal including any one of an instruction, a data, a position where the data exists, or a timing signal (see col. 5, lines 19-22; and an output terminal (output port 120 of fig. 1) for producing a signal formed by an internal circuit (150 and 121 of fig. 1) in response to the input signal (see col. 5, lines 2-5).

Regarding claim 2, Hansen et al. further disclose the instruction being a command for specifying the state of operation; the data being the one to be stored; the position where the data exists is an address signal; the timing signal being a clock (see col. 5, line 20); and the semiconductor integrated circuit device including a memory circuit that operates in response to a command and an address signal input in synchronism with the clock (see col. 11, lines 32-35).

Regarding claim 3, Hansen et al. further disclose the memory circuit replacing the stored data read out according to the address by the input data through the input terminal and producing the input data from the output terminal when it has received a reading operation instruction corresponding to the address assigned thereto (see col. 7, lines 52-60).

Regarding claim 7, Hansen et al. disclose in figs. 1 and 5, a plurality of semiconductor integrated circuit devices each having an input terminal (110 of fig. 1) for receiving an input signal containing any one of an instruction, a data, a position where the data exists or a timing signal, and an output terminal (120 of fig. 1) for producing a signal formed in an internal circuit in response to the input signal; and a signal-forming circuit for forming an input signal containing any one of the instruction, the data, the position where the data exists or the timing signal for the semiconductor integrated circuit devices (see col. 5, lines 19-22); wherein the

output terminal of the semiconductor integrated circuit device in the preceding stage and the corresponding input terminal of the semiconductor integrated circuit device of the next stage are connected in cascade (see fig. 5); the input signal containing any one of the instruction, the data, the position where the data exists or the timing signal formed by the signal-forming circuit is fed to the input terminal of the semiconductor integrated circuit device of the initial stage in the cascade connection (see fig. 5); and among the signals from the output terminal of the semiconductor integrated circuit device of the final stage in the cascade connection, at least the signal corresponding to the data is transmitted to the signal-processing circuit (500 of fig. 5).

Regarding claim 8, Hansen et al. further disclose the instruction being a command for specifying the state of operation; the data is the one to be stored; the position where the data exists is an address signal; the timing signal is a clock (see col. 5, line 20); and each of the plurality of semiconductor integrated circuit devices includes a memory circuit that operates in response to a command and an address signal input in synchronism with the clock (see col. 11, lines 32-35).

Regarding claim 10, Hansen et al. disclose in figs. 1 and 5, a plurality of semiconductor memory devices each having an input terminal (input port 110) for receiving an input signal containing any one of a command, a data, an address or a timing signal (see fig. 1), and an output terminal (output port 120) for producing a signal corresponding to the input signal fed through the input terminal, wherein among the plurality of semiconductor memory devices, the output terminal of the semiconductor memory device in the preceding stage and the corresponding input terminal of the semiconductor memory device of the next stage are connected in cascade (see fig. 5).

Regarding claim 11, Hansen et al. further disclose the input terminal of the semiconductor memory device of the initial stage in cascade receives the command, the data (see fig. 5), the address or the timing signal formed by the signal-forming circuit (host 500 of fig. 5), and among the output signals produced from the output terminal of the semiconductor memory device in the final stage in cascade, at least a signal corresponding to the data is transmitted to the signal-forming circuit (see fig. 5).

Regarding claim 12, Hansen et al. further disclose the signal-forming circuit (500 of fig. 5) being a memory control device constituted by a semiconductor integrated circuit device (see fig. 5).

Regarding claim 15, Hansen et al. further disclose the data formed by the memory control device being delivered to the input terminals of the plurality of semiconductor memory devices constituting the initial stage, and a plurality of semiconductor memory devices being provided from a next stage up to the final stage being corresponded to the plurality of semiconductor memory devices in the initial stage and are connected in cascade being corresponded thereto in a one-to-one manner (see fig. 5).

Regarding claim 16, Hansen et al. further disclose the command and the address formed by the signal-forming circuit (500 of fig. 5) being transmitted in common to the input terminals of the plurality of semiconductor memory devices constituting the initial stage, and the command and the address being connected in a one-to-one manner being corresponded to the data in the connection of from the output terminals of the plurality of semiconductor memory devices in the initial stage up to the input terminals of the plurality of semiconductor memory devices in the final stage (see fig. 5).

Regarding claim 17, Hansen et al. further disclose the signal-forming circuit forming a plurality of sets of commands and addresses corresponding to the input terminals of the plurality of semiconductor memory devices constituting the initial stage (see fig. 1), and transmitting them to the input terminals of the plurality of semiconductor memory devices constituting the initial stage in a one-to-one matter (see fig. 2 and col. 5, lines 35-48); and the commands and addresses being connected in a one-to-one manner being corresponded to the data even in the connections of from the output terminals of the plurality of semiconductor memory devices in the initial stage up to the input terminals of the plurality of semiconductor memory devices in the final stage (see fig. 5).

Regarding claim 18, Hansen et al. further disclose the plurality of semiconductor memory devices replacing stored data read out according to the address by the input data through the input terminals and producing the input data from the output terminals when they have received a reading operation instruction corresponding to the addresses assigned thereto (see col. 7, lines 17-36).

Regarding claim 19, Hansen et al. further disclose the semiconductor memory devices in the preceding stage and the semiconductor memory devices in the succeeding stage to be connected in cascade (see fig. 5) being mounted on the front surface and on the back surface of a common mounting board, and being connected in cascade via the through holes (see fig. 5).

Regarding claim 20, Hansen et al. further disclose the semiconductor memory devices having a buffer circuit (402 of fig. 4) for reading (see col. 7, lines 57-60), wherein the buffer circuit includes a first reading command for reading the stored data from the memory cells and for holding the data in the buffer circuit for reading and a second reading command for

producing, from the output terminals, the stored data held in the buffer circuit for reading (see col. 7, lines 52-65).

Regarding claim 21, Hansen et al. further disclose the semiconductor memory devices having a buffer circuit for writing (401 of fig. 4 and see col. 7, lines 55-60), the write command writes the data fed from the external terminals into the buffer for writing, and the data written into the buffer for writing are autonomously written into the memory cells by the internal control circuit (see col. 7, lines 52-67).

Regarding claim 22, Hansen et al. further disclose the data being such that among the transmission lines of a number of m, the transmission lines of a number of at least n transit the level periodically (see col. 5, lines 20-35).

Allowable Subject Matter

7. Claims 4-6, 9, and 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest a device having the data and the timing signal output from the output terminal being re-adjusted by a timing signal produced therein as recited in claims 4, 9 and 13.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fumaba et al. (US. 6,519,173) disclose the connection of a plurality of memory chips in a memory system.

Kawaguchi et al. (US. 6,098,159) disclose an information processing apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Le whose telephone number is (571) 272-1872. The examiner can normally be reached on M-F (8.00AM - 5.30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TL
October 2, 2006

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